



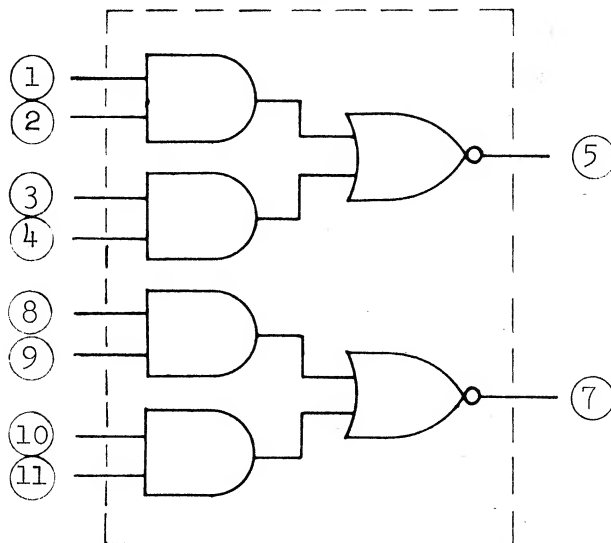
Preliminary Specifications

DESCRIPTION

The SN676 is a dual TTL Exclusive OR gate with low propagation delay and high noise immunity designed to operate over the full military temperature range of -55°C to +125°C. The SN676 is fabricated using diffused planar epitaxial techniques.

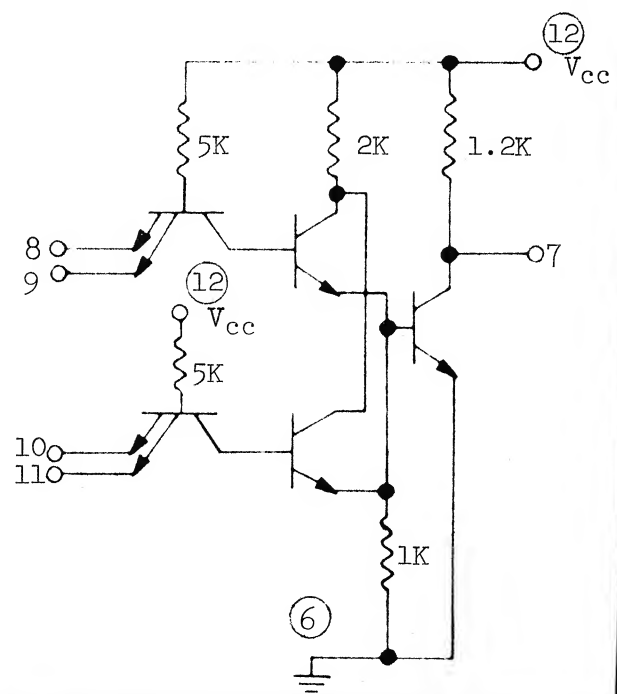
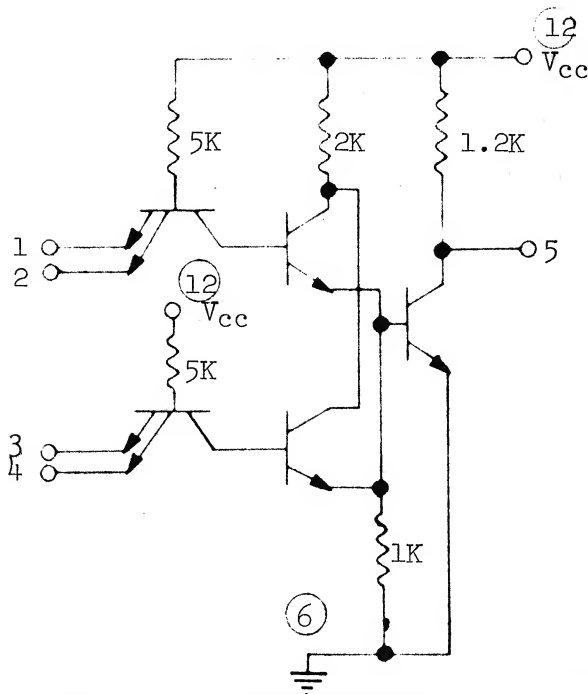
August 1964

LOGIC DIAGRAMS



	Positive	Negative
5	$(1)(2) + (3)(4)$	$(1+2)(3+4)$
7	$(8)(9) + (10)(11)$	$(8+9)(10+11)$

NETWORK CIRCUIT DIAGRAMS



Preliminary Specifications

NETWORK CHARACTERISTICS

Absolute Maximum Ratings:

Supply Voltage	8 volts
Input Voltage	6 volts
Output Voltage	8 volts
Power Dissipation	200 mw
Operating Temperature	-55°C to +125°C

Network Electrical Characteristics

Network Parameters										MIN	MAX	UNIT
Operating Supply Voltage										4.0	5.0	v
Fan-Out: Each Output Paralleled Output											7 5	
Off Voltage	PIN	1	2	3	4	8	9	10	11			
$V_{cc} = 4.0$ volts Temperature +125°C (See Figure 1)	5	0.8	4.5	0.8	4.5	-	-	-	-	2.3		v
	5	4.5	0.8	0.8	4.5	-	-	-	-	2.3		v
	5	0.8	4.5	4.5	0.8	-	-	-	-	2.3		v
	5	4.5	0.8	4.5	0.8	-	-	-	-	2.3		v
	7	-	-	-	-	0.8	4.5	0.8	4.5	2.3		v
	7	-	-	-	-	4.5	0.8	0.8	4.5	2.3		v
	7	-	-	-	-	0.8	4.5	4.5	0.8	2.3		v
	7	-	-	-	-	4.5	0.8	4.5	0.8	2.3		v
Saturation Voltage	PIN	1	2	3	4	8	9	10	11			
$V_{cc} = 4.0$ volts (See Figure 3)	(+125°C	5	0	-	2.0	2.0	-	-	-	-	0.5	v
	(5	2.0	2.0	0	-	-	-	-	-	0.5	v
	(7	-	-	-	-	0	-	2.0	2.0	0.5	v
	(7	-	-	-	-	2.0	2.0	0	-	0.5	v
	(-55°C	5	0	-	2.0	2.0	-	-	-	-	0.5	v
	(5	2.0	2.0	0	-	-	-	-	-	0.5	v
	(7	-	-	-	-	0	-	2.0	2.0	0.5	v
	(7	-	-	-	-	2.0	2.0	0	-	0.5	v
Input Short Current	PIN	1	2	3	4	8	9	10	11			
$V_{cc} = 4.5$ volts Temperature +125°C (See Figure 2)	1	0	4.5	-	-	-	-	-	-		1.2	ma
	3	-	-	0	4.5	-	-	-	-		1.2	ma
	8	-	-	-	-	0	4.5	-	-		1.2	ma
	10	-	-	-	-	-	-	0	4.5		1.2	ma
Noise Immunity										300		mv

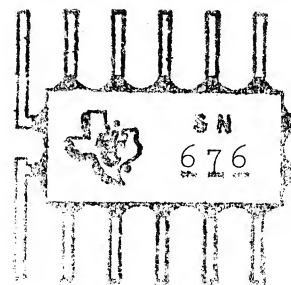


Preliminary Specifications

NETWORK PARAMETERS										MIN	MAX	UNIT
Output Short Current (See Figure 4) $V_{CC} = 4.5 \text{ v}$	PIN	1	2	3	4	8	9	10	11			
		5	0	0	0	0	-	-	-		4.0	ma
		7	-	-	-	-	0	0	0		4.0	ma
		5	0	0	0	0	-	-	-	2.5		ma
-55°C		7	-	-	-	-	0	0	0	2.5		ma
Input Leakage Current Temperature +125°C $V_{CC} = 4.5 \text{ v}$ (See Figure 5)	PIN	1	2	3	4	8	9	10	11			
		1	4.5	0	-	-	-	-	-		100	µa
		2	0	4.5	-	-	-	-	-		100	µa
		3	-	-	4.5	0	-	-	-		100	µa
		4	-	-	0	4.5	-	-	-		100	µa
		8	-	-	-	-	4.5	0	-		100	µa
		9	-	-	-	-	0	4.5	-		100	µa
		10	-	-	-	-	-	-	4.5		100	µa
		11	-	-	-	-	-	0	4.5		100	µa
On Current (from V_{CC}) $V_{CC} = 5.0 \text{ v}$ 5.0 volts on all inputs; outputs open Temperature +125°C											20	ma
Off Current (from V_{CC}) $V_{CC} = 5.0 \text{ v}$ 0 volts on all inputs; outputs open Temperature +125°C											8	ma
Leading Edge Delay ($\frac{T_+}{2}$) $V_{CC} = 4.0 \text{ v}$ (See Figure 6)	PIN	1	2	3	4	8	9	10	11			
		1	4.0	0	-	pin 5	4.0	0	-		35	ns
		2	4.0	0	-	pin 5	4.0	0	-		35	ns
		3	0	-	4.0	0	-	pin 5	4.0		35	ns
Trailing Edge Delay ($\frac{T_-}{2}$) $V_{CC} = 4.0 \text{ v}$ (See Figure 6)	PIN	1	2	3	4	8	9	10	11			
		1	4.0	0	-	pin 5	4.0	0	-		35	ns
		2	4.0	0	-	pin 5	4.0	0	-		35	ns
		3	0	-	4.0	0	-	pin 5	4.0		35	ns
		4	0	-	4.0	0	-	pin 5	4.0		35	ns

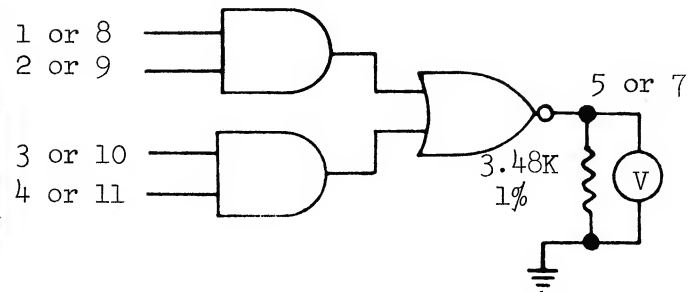


12 11 10 9 8 7

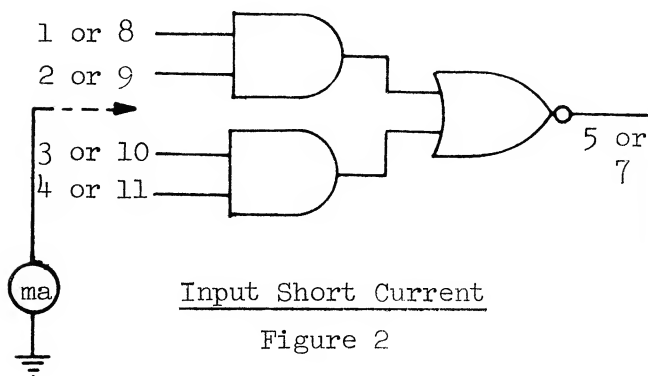


1 2 3 4 5 6

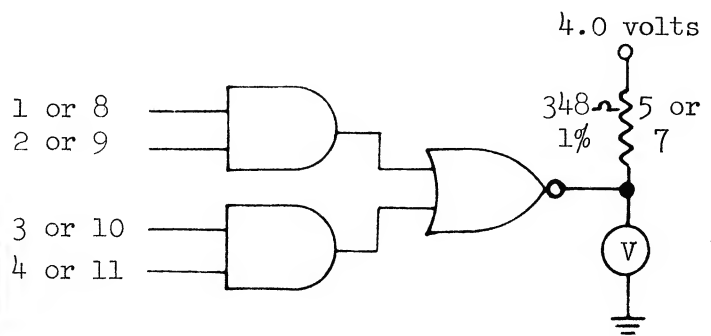
Package



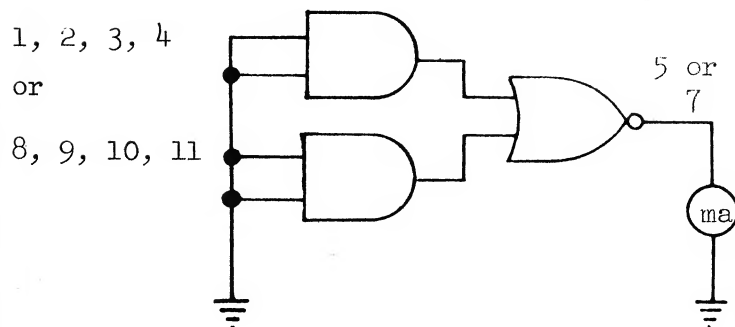
Off Voltage
Figure 1



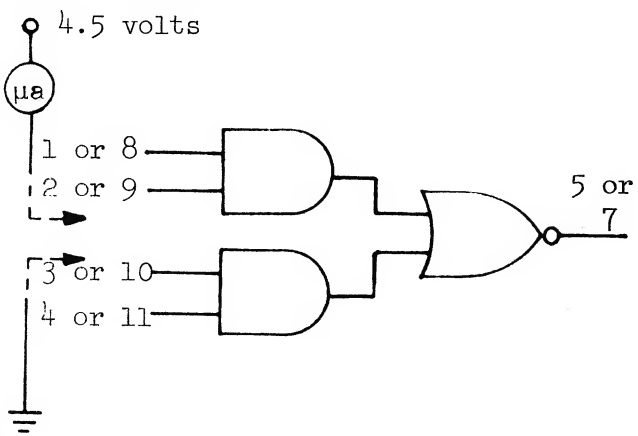
Input Short Current
Figure 2



Saturation Voltage
Figure 3



Output Short Current
Figure 4

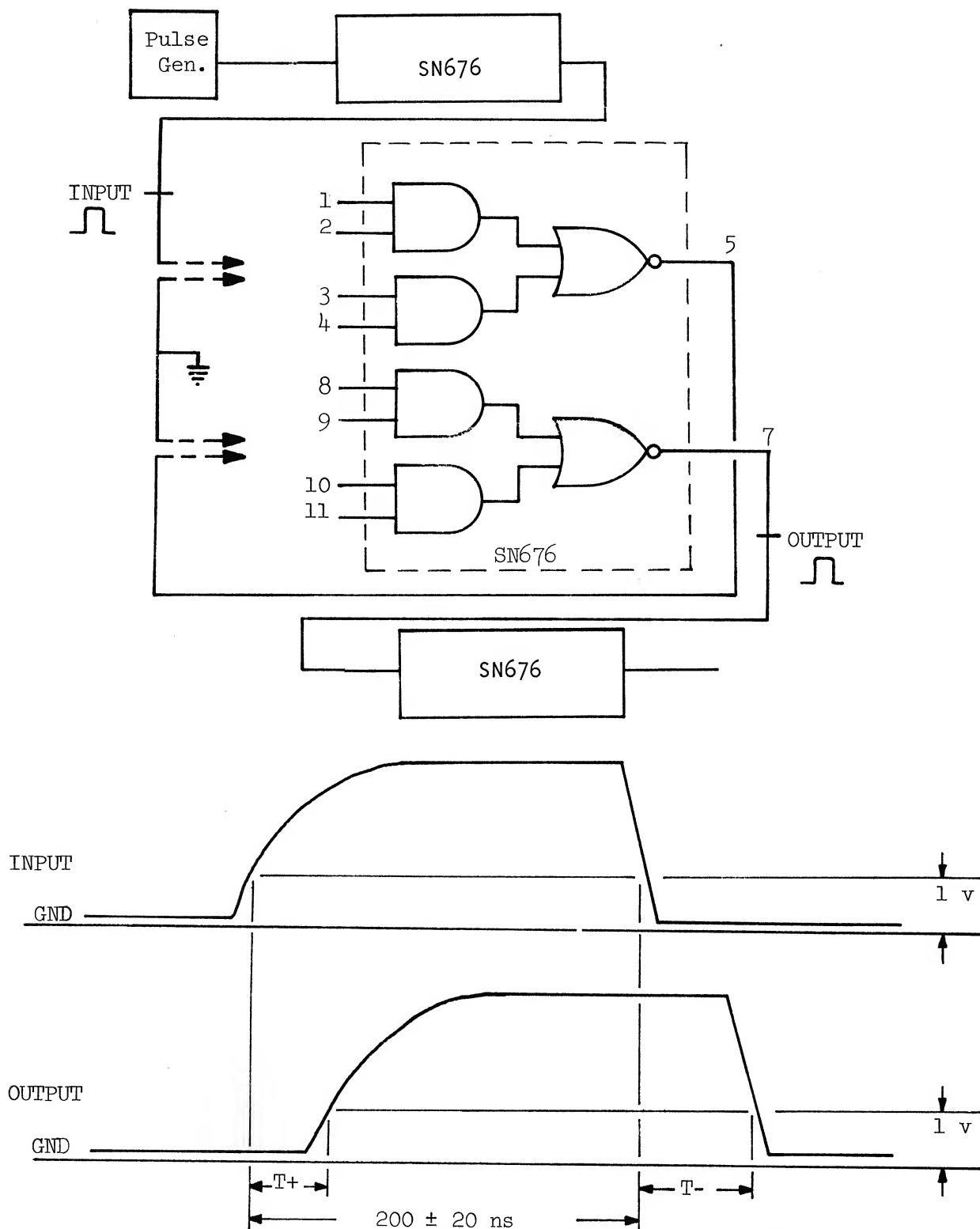


Input Leakage Current
Figure 5



PROPAGATION DELAY

Figure 6



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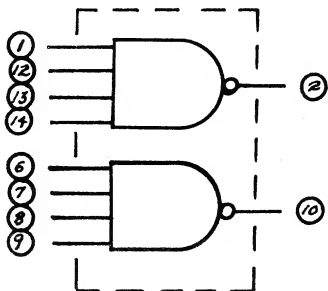
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Description

The SN742 is a dual, 4-input, TTL, positive NAND gate capable of driving large fan-out and high capacity loads over the full military temperature range of -55°C to +125°C. The SN742 is fabricated using diffused planar double epitaxial techniques.

Logic DiagramLogic

Positive NAND:

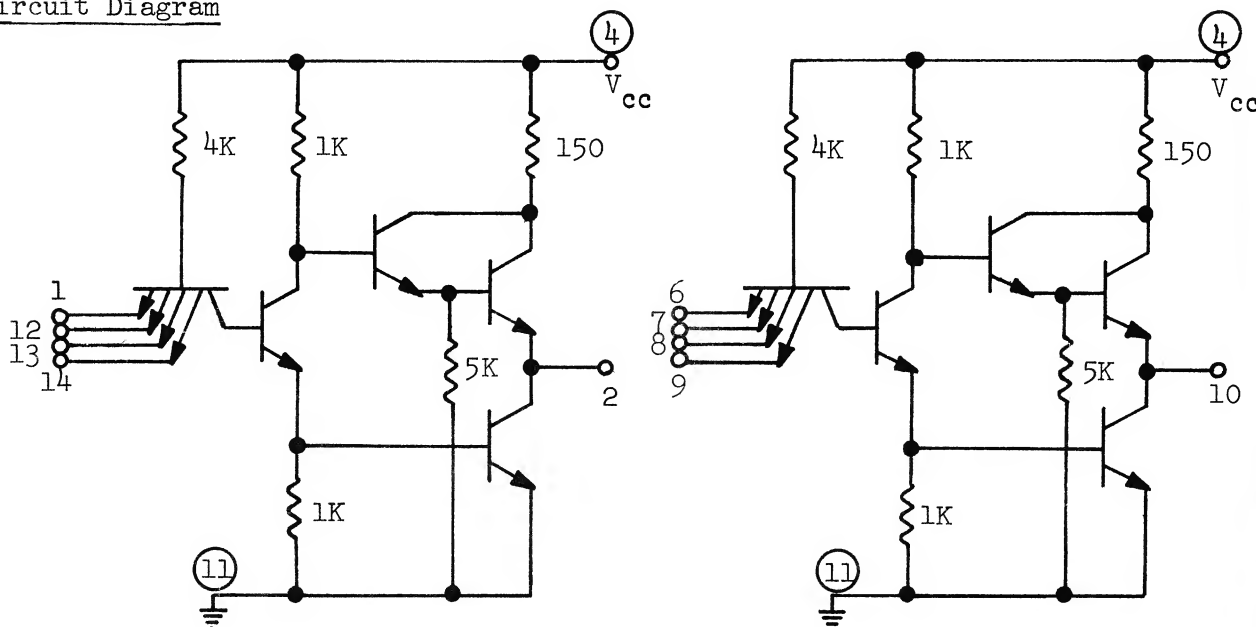
$$2 = \overline{(1)(2)(3)(4)}$$

$$10 = \overline{(6)(7)(8)(9)}$$

Negative NOR:

$$2 = \overline{1+2+3+4}$$

$$10 = \overline{6+7+8+9}$$

Circuit DiagramTypical Electrical Characteristics

Fan-out	15
Propagation Delay	25 ns
Noise Margin	600 mv
Power Dissipation	15 mw

August 1964



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PRELIMINARY SPECIFICATIONS

NETWORK CHARACTERISTICS

Absolute Maximum Ratings:

Supply Voltage	8 volts
Input Voltage	6 volts
Operating Ambient Temperature Range	-55°C to +125°C
Storage Temperature	-65°C to +150°C

All data applies for the following conditions unless otherwise noted:

Temperature: -55°C to +125°C
 Fan-Out: 1 to 15
 $V_{CC} = 4.5$ volts

NETWORK PARAMETERS										MIN	MAX	UNIT
Operating Supply Voltage										4.5	5.5	v
Fan-Out										1	15	
Output ON Level $I_{10} = I_2 = 20\text{ma}$ (See Figure 1)	PIN	1	12	13	14	6	7	8	9			
	(2	-	-	-	-	-	-	-	-		0.5	v
	(10	-	-	-	-	-	-	-	-			
	(2	2.0	2.0	2.0	2.0	-	-	-	-		0.5	v
Output OFF Level $I_{10} = I_2 = -2\text{ma}$ (See Figure 2)	(10	-	-	-	-	2.0	2.0	2.0	2.0		0.5	v
	(2	0.8	-	-	-	-	-	-	-	2.4		v
	(2	-	0.8	-	-	-	-	-	-	2.4		v
	(2	-	-	0.8	-	-	-	-	-	2.4		v
Output OFF Level $I_{10} = I_2 = -2\text{ma}$ (See Figure 2)	(2	-	-	-	0.8	-	-	-	-	2.4		v
	(10	-	-	-	-	0.8	-	-	-	2.4		v
	(10	-	-	-	-	-	0.8	-	-	2.4		v
	(10	-	-	-	-	-	-	0.8	-	2.4		v
	(10	-	-	-	-	-	-	-	0.8	2.4		v
	(2	0.8	-	-	-	-	-	-	-	2.4		v
	(10	-	-	-	-	0.8	-	-	-	2.4		v
	(10	-	-	-	-	-	-	-	0.8	2.4		v
Noise Immunity (Output ON Level)										300		mv
(Output OFF Level)										400		mv
Input Current $V_{CC} = 5.5$ volts (See Figure 4)	PIN	1	12	13	14	6	7	8	9			
	12	4.5	0	4.5	4.5	-	-	-	-		-1.6	ma
	13	4.5	4.5	0	4.5	-	-	-	-		-1.6	ma
	7	-	-	-	-	4.5	0	4.5	4.5			
											-1.6	ma

NETWORK PARAMETERS										MIN	MAX	UNIT
Input Leakage Current $V_{cc} = 5.5$ volts (See Figure 3)	PIN	1	12	13	14	6	7	8	9			
	1	4.5	0	0	0	-	-	-	-		150	ua
	12	0	4.5	0	0	-	-	-	-		150	ua
	13	0	0	4.5	0	-	-	-	-		150	ua
	14	0	0	0	4.5	-	-	-	-		150	ua
	6	-	-	-	-	4.5	0	0	0		150	ua
	7	-	-	-	-	0	4.5	0	0		150	ua
	8	-	-	-	-	0	0	4.5	0		150	ua
	9	-	-	-	-	0	0	0	4.5		150	ua
	1	5.5	0	0	0	-	-	-	-		1.0	ma
	12	0	5.5	0	0	-	-	-	-		1.0	ma
	13	0	0	5.5	0	-	-	-	-		1.0	ma
	14	0	0	0	5.5	-	-	-	-		1.0	ma
	6	-	-	-	-	5.5	-	-	-		1.0	ma
	7	-	-	-	-	0	5.5	0	0		1.0	ma
	8	-	-	-	-	0	0	5.5	0		1.0	ma
	9	-	-	-	-	0	0	0	5.5		1.0	ma
Short Current (See Fig. 5) $V_{cc} = 5.5$ volts Pins 2 and 10 = 0 volts	PIN	1	12	13	14	6	7	8	9			
	2	0	-	-	-	-	-	-	-	-20	-45	ma
	10	-	-	-	-	0	-	-	-	-20	-45	ma
Power Drain (From V_{cc}) $V_{cc} = 5.5$ volts	PIN	1	12	13	14	6	7	8	9			
	4	0	-	-	-	0	-	-	-		6	ma
	4	-	-	-	-	-	-	-	-		12	ma
Current (I_{μ}) of Breakdown Voltage ($V_{cc} = 8$ volts) Pins 1 and 6 = 0 volts Temperature 25°C											12	ma

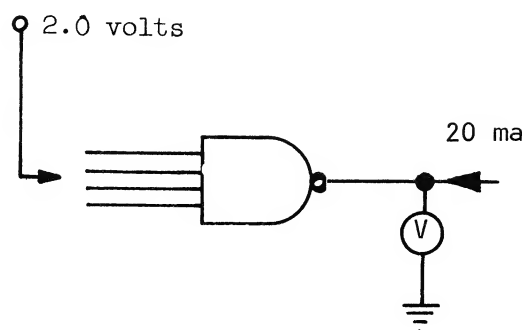
SWITCHING TIME			MIN	MAX	UNIT
Delay Time (t_d) Fan-Out = 15	(See Figure 7)	C = 100 pf		50	ns
		C = 500 pf		80	ns
Rise Time (t_r) Fan-Out = 1 and 15	(See Figure 7)	C = 100 pf		45	ns
		C = 500 pf		70	ns
Fall Time (t_f) Fan-Out = 15	(See Figure 7)	C = 100 pf		35	ns
		C = 500 pf		50	ns
Storage Time (t_s) Fan-Out	(See Figure 7)	C = 100 pf		65	ns
		C = 500 pf		100	ns



(R)

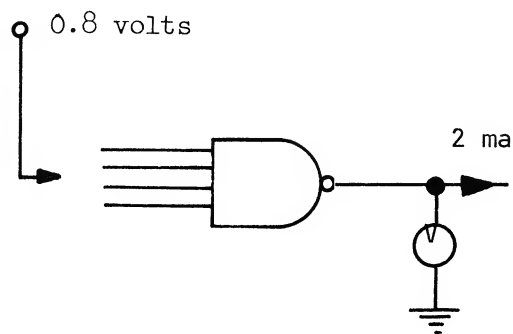
SOLID CIRCUIT
TYPE SN742
DUAL NAND GATE

PRELIMINARY SPECIFICATIONS



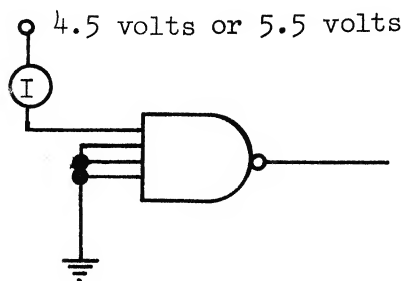
Output On Level

Fig. 1



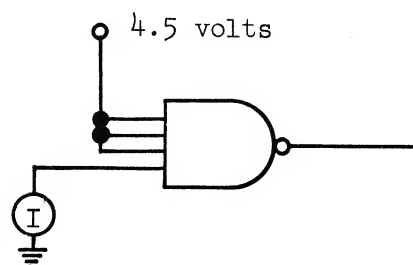
Output Off Level

Fig. 2



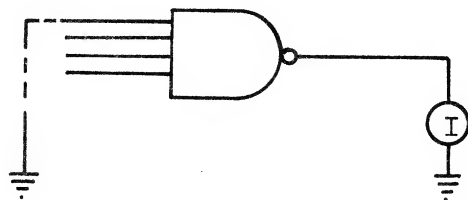
Input Leakage Current

Fig. 3



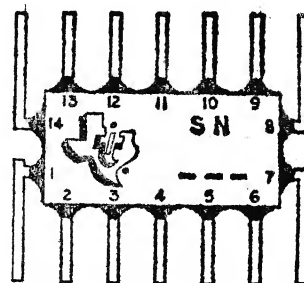
Input Current

Fig. 4



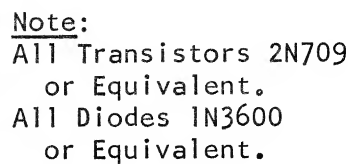
Short Current

Fig. 5



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SOLID CIRCUIT
TYPE SN742
DUAL NAND GATE

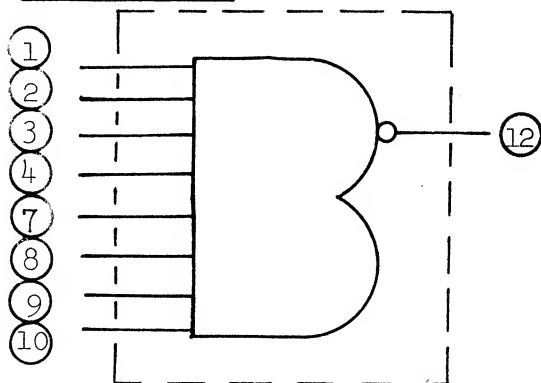




August 1964

DESCRIPTION

The SN743 is an 8-input, TTL, positive NAND gate capable of driving large fan-out and high capacity loads over the full military temperature range of -55°C to $+125^{\circ}\text{C}$. The SN743 is fabricated using diffused planar double epitaxial techniques.

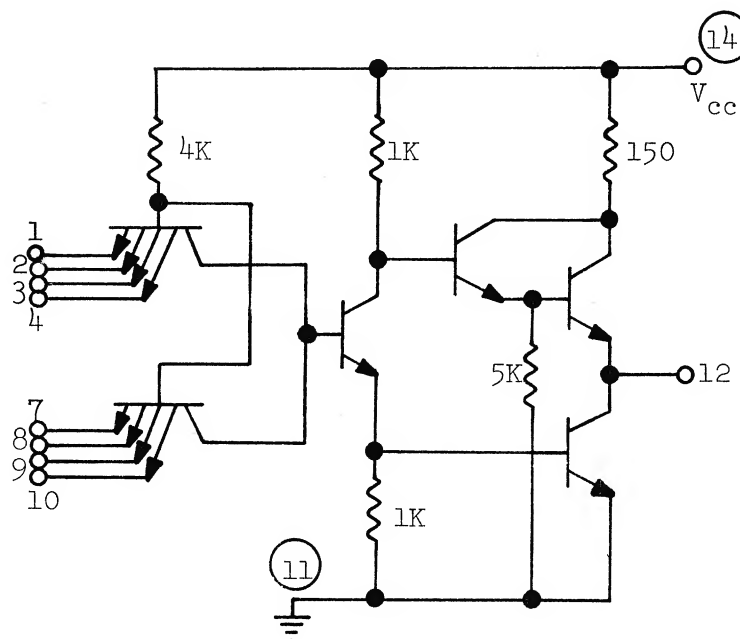
LOGIC DIAGRAMLOGIC

Positive NAND:

$$12 = \overline{(1)(2)(3)(4)(7)(8)(9)(10)}$$

Negative NOR:

$$12 = \overline{1+2+3+4+7+8+9+10}$$

CIRCUIT DIAGRAMTYPICAL ELECTRICAL CHARACTERISTICS

Fan-out	15
Propagation	25 ns
Noise Margin	600 mv
Power Dissipation	15 mw



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PRELIMINARY SPECIFICATIONS

NETWORK CHARACTERISTICS

Absolute Maximum Ratings:

Supply Voltage	8 volts
Input Voltage	6 volts
Operating Ambient Temperature Range	-55°C to +125°C
Storage Temperature	-65°C to +150°C

Network Electrical Characteristics

All data applies for the following conditions unless otherwise noted:

Temperature: -55°C to +125°C

Fan-Out: 1 to 15

$V_{CC} = 4.5$ volts

NETWORK PARAMETERS										MIN	MAX	UNIT
Operating Supply Voltage										4.5	5.5	v
Fan-Out										1	15	
Output ON Level (See Fig.1)												
$V_{CC} = 4.5$ v $I_{12} = 20$ ma	PIN	1	2	3	4	7	8	9	10			
	12	-	-	-	-	-	-	-	-		0.5	v
	12	2.0	2.0	2.0	2.0	2.0	2.0	2.0	2.0		0.5	v
Output OFF Level												
$V_{CC} = 4.5$ v $I_{12} = -2$ ma (See Figure 2)	(PIN	1	2	3	4	7	8	9	10			
	(12	0.8	-	-	-	-	-	-	-	2.4		v
	(12	-	0.8	-	-	-	-	-	-	2.4		v
	(12	-	-	0.8	-	-	-	-	-	2.4		v
	(12	-	-	-	0.8	-	-	-	-	2.4		v
	(12	-	-	-	-	0.8	-	-	-	2.4		v
	(12	-	-	-	-	-	0.8	-	-	2.4		v
	(12	-	-	-	-	-	-	0.8	-	2.4		v
	(12	-	-	-	-	-	-	-	0.8	2.4		v
	(12	0.8	-	-	-	-	-	-	-	2.4		v
Noise Immunity (Output ON Level)										300		mv
(Output OFF Level)										400		mv
Input Current												
(See Figure 4) $V_{CC} = 5.5$ v												
	4	4.5	4.5	4.5	0	4.5	4.5	4.5	4.5		-1.6	ma
Short Current (See Fig.5)												
$V_{CC} = 5.5$ v; Pin 12 = 0 v												
	12	0	-	-	-	-	-	-	-	-20	-45	ma



PRELIMINARY SPECIFICATIONS

SOLID CIRCUIT ^(R)
 TYPE SN742
 DUAL NAND GATE

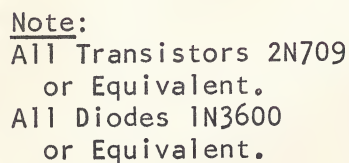
NETWORK PARAMETERS										MIN	MAX	UNIT
Input Leakage Current $V_{cc} = 5.5$ volts (See Figure 3)	PIN	1	12	13	14	6	7	8	9			
	1	4.5	0	0	0	-	-	-	-		150	ua
	12	0	4.5	0	0	-	-	-	-		150	ua
	13	0	0	4.5	0	-	-	-	-		150	ua
	14	0	0	0	4.5	-	-	-	-		150	ua
	6	-	-	-	-	4.5	0	0	0		150	ua
	7	-	-	-	-	0	4.5	0	0		150	ua
	8	-	-	-	-	0	0	4.5	0		150	ua
	9	-	-	-	-	0	0	0	4.5		150	ua
	1	5.5	0	0	0	-	-	-	-		1.0	ma
	12	0	5.5	0	0	-	-	-	-		1.0	ma
	13	0	0	5.5	0	-	-	-	-		1.0	ma
	14	0	0	0	5.5	-	-	-	-		1.0	ma
	6	-	-	-	-	5.5	-	-	-		1.0	ma
	7	-	-	-	-	0	5.5	0	0		1.0	ma
	8	-	-	-	-	0	0	5.5	0		1.0	ma
	9	-	-	-	-	0	0	0	5.5		1.0	ma
Short Current (See Fig. 5) $V_{cc} = 5.5$ volts Pins 2 and 10 = 0 volts	PIN	1	12	13	14	6	7	8	9			
	2	0	-	-	-	-	-	-	-	-20	-45	ma
	10	-	-	-	-	0	-	-	-	-20	-45	ma
Power Drain (From V_{cc}) $V_{cc} = 5.5$ volts	PIN	1	12	13	14	6	7	8	9			
	4	0	-	-	-	0	-	-	-		6	ma
	4	-	-	-	-	-	-	-	-		12	ma
Current (I_H) of Breakdown Voltage ($V_{cc} = 8$ volts) Pins 1 and 6 = 0 volts Temperature 25°C											12	ma

SWITCHING TIME				MIN	MAX	UNIT
Delay Time (t_d) Fan-Out = 15	(See Figure 7)	C = 100 pf			50	ns
		C = 500 pf			80	ns
Rise Time (t_r) Fan-Out = 1 and 15	(See Figure 7)	C = 100 pf			45	ns
		C = 500 pf			70	ns
Fall Time (t_f) Fan-Out = 15	(See Figure 7)	C = 100 pf			35	ns
		C = 500 pf			50	ns
Storage Time (t_s) Fan-Out	(See Figure 7)	C = 100 pf			65	ns
		C = 500 pf			100	ns



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 POST OFFICE BOX 5012 • DALLAS 22, TEXAS

SOLID CIRCUIT
TYPE SN742
DUAL NAND GATE



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